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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/068,879	02/11/2002	Keijiro Naito	111938	1409

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OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER

SHANKAR, VIJAY

ART UNIT	PAPER NUMBER
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2673

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/068,879	Applicant(s) NAITO, KEIJIRO	
	Examiner VIJAY SHANKAR	Art Unit 2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 January 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 17 and 18 is/are allowed.
- 6) ☒ Claim(s) 1-4, 8, 12, 16, 19 and 20 is/are rejected.
- 7) ☒ Claim(s) 5-7, 9-11 and 13-15 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4, 8, 12, 16, 19-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Hoshi (4,455,576).

Regarding Claim 1, Hoshi teaches a liquid crystal device (Fig.4) having multiple pixels (fig.4), the liquid crystal device comprising: an input terminal that receives a display signal including a predetermined signal used for generating a common signal and multiple pixel signals to be supplied to the multiple pixels (Figs.4,7; Column 2, line 63- Col.3, line 20), wherein the predetermined signal is embedded into a predetermined period between a group of pixel signals and another group of pixel signals in the display signal, and the common signal is to be commonly supplied to the multiple pixels. (Figs.4,7; Column 2, line 63- Col.3, line 20; Col.3, line 31- Col.4, line 60).

Regarding Claims 2,3, Hoshi teaches a liquid crystal device wherein the predetermined period is part of a horizontal scanning period except an effective horizontal scan period, and the predetermined period is part of a vertical scanning period except an effective vertical scan period. (Figs.4,7,15; Col.3, line 31- 67; Col.5, line 16- Col.6, line 20).

Regarding Claim 4,8, 12, Hoshi teaches a liquid crystal device the liquid crystal device further comprising: a common signal line that is commonly connected to the multiple pixels; and a common signal line driving circuit that generates the common signal in response to the predetermined signal included in the display signal input from the input terminal and supplies the generated common signal to the common signal line. (Figs.4,7; Column 2, line 63- Col.3, line 20; Col.3, line 31- Col.4, line 60).

Regarding Claim 16, Hoshi teaches an image processing device that generates a display signal, which is to be input into a liquid crystal device having multiple pixels (Figs.4,7; Column 2, line 63- Col.3, line 20), the image processing device comprising: a video signal conversion circuit that converts an input video signal and generates multiple pixel signals, which are to be given to the multiple pixels of the liquid crystal device(Figs.4,7; Col.3, line 31- Col.4, line 60; fig.13; Col.5, line 15- Col.6, line 59); and a display signal generation circuit that combines the multiple pixel signals with a predetermined signal, which is used for generating a common signal to be commonly

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supplied to the multiple pixels, and thereby generates one display signal. (Figs.4,7; Column 2, line 63- Col.3, line 20; Col.3, line 31- Col.4, line 60).

Regarding Claim 19, Hoshi teaches a method of inputting a predetermined signal into a liquid crystal device that has multiple pixels and receives a display signal including multiple pixel signals, which are to be given to the multiple pixels, the predetermined signal being used for generating a common signal to be commonly supplied to the multiple pixels (Figs.4,7; Column 2, line 63- Col.3, line 20), the method comprising the step of: embedding the predetermined signal into a predetermined period between a group of pixel signals and another group of pixel signals in the display signal and inputting the embedded predetermined signal as part of the display signal. (Figs.4,7; Column 2, line 63- Col.3, line 20; Col.3, line 31- Col.4, line 60).

Regarding Claim 20, Hoshi teaches an image processing method that generates a display signal, which is to be input into a liquid crystal device having multiple pixels, the image processing method comprising the steps of: converting an input video signal and generating multiple pixel signals, which are to be given to the multiple pixels of the liquid crystal device (Figs.4,7; Column 2, line 63- Col.3, line 20); and combining the multiple pixel signals with a predetermined signal, which is used for generating a common signal to be commonly supplied to the multiple pixels, and thereby generating one display signal. (Figs.4,7; Column 2, line 63- Col.3, line 20; Col.3, line 31- Col.4, line 60).

Allowable Subject Matter

4. Claims 17-18 are allowed.
5. Claims 5-7, 9-11, 13-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
6. The following is an examiner's statement of reasons for allowance: The present invention is directed to a liquid crystal device wherein the common signal line driving circuit is a sample/hold circuit that samples the predetermined signal included in the display signal input from the input terminal and outputs the predetermined sampled signal as the common signal as claimed in Claim 5, 9, 13.

The present invention is directed to the liquid crystal device further comprising: multiple rows of scanning lines and multiple columns of signal lines for selecting the multiple pixels; a scanning line driving circuit that supplies scanning signals to the corresponding multiple rows of scanning lines in a sequence of the multiple rows of scanning lines; and a signal line driving circuit that samples display signals corresponding to the multiple columns of signal lines in a sequence of the multiple columns of signal lines and supplies the sampled display signals to the corresponding signal lines, wherein the signal line driving circuit supplies a sample/hold signal, which is used for sampling the predetermined signal, to the common signal line driving circuit as claimed in Claims 6,10,14.

The present invention is directed to the liquid crystal device further comprising: multiple rows of scanning lines and multiple columns of signal lines for selecting the multiple pixels; a scanning line driving circuit that supplies scanning signals to the corresponding multiple rows of scanning lines in a sequence of the multiple rows of scanning lines; and a signal line driving circuit that samples display signals corresponding to the multiple columns of signal lines in a sequence of the multiple columns of signal lines and supplies the sampled display signals to the corresponding signal lines, wherein the scanning line driving circuit supplies a sample/hold signal, which is used for sampling the predetermined signal, to the common signal line driving circuit as claimed in Claims 7,11,15.

The present invention is directed to an image display apparatus, comprising: a liquid crystal device having multiple pixels; and an image processing device that generates a display signal, which is to be input into the liquid crystal device, the liquid crystal device comprising: an input terminal that receives the display signal including a predetermined signal used for generating a common signal and multiple pixel signals to be supplied to the multiple pixels, wherein the predetermined signal is embedded into a predetermined period between a group of pixel signals and another group of pixel signals in the display signal, and the common signal is to be commonly supplied to the multiple pixels, the image processing device comprising: a video signal conversion circuit that converts an input video signal and generates the multiple pixel signals, which are to be given to the multiple pixels of the liquid crystal device; and a display signal

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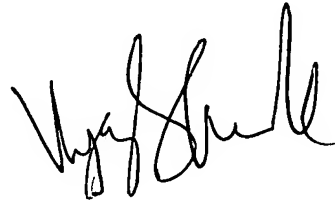
generation circuit that combines the multiple pixel signals with a predetermined signal, which is used for generating a common signal to be commonly supplied to the multiple pixels, and thereby generates one display signal as claimed in Claim 17.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VIJAY SHANKAR whose telephone number is (571) 272-7682. The examiner can normally be reached on M-F 7:00 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, BIPIN SHALWALA can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Vijay Shankar', with a stylized, cursive script.

VIJAY SHANKAR
Primary Examiner
Art Unit 2673

VS